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(71) Applicant: Xilinx, Inc.
2069 E. Hamilton Avenue
San Jose California 95125(US)

(72) Inventor: Freeman, Ross H.
5667 McKellar Drive
San Jose California 95129(US)

(74) Representative: Noz, Franciscus Xaverius, Ir. et al,
Boschdijk 155 P.O. Box 645
NL-5600 AP Eindhoven(NL)

10.2.88 Peterborough

(54) Configurable logic array.

(57) The shift register comprises
a plurality of dynamic storage cells 1 through K connected in series where K is a selected integer representing the maximum number of storage cells in series.
means for transferring data sequentially from one cell to the next cell so as to fill all the cells of the shift register, and
means for holding the data in each cell indefinitely.

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CONFIGURABLE LOGIC ARRAY

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to programmable logic arrays and in particular, to a method for providing on-chip programming of each of a plurality of logic elements formed on a chip of semiconductor material to configure each logic element to carry out certain desired functions.

Prior Art

Gate arrays are well known in the prior art. Typically a gate array is produced by interconnecting a plurality of active devices in a base array in any one of a number of ways to achieve a desired logic function. As gate arrays become more complex, the simulation of the logic to be achieved from a given interconnection of the active devices in the base array becomes more difficult and is typically carried out using a computer program. The layout of the actual interconnections for the active devices in the base array to yield a finished gate array is then derived using a computer aided design program of

a type well known in the art. The process of designing such a structure is complex and reasonably expensive requiring the use of logic simulation and verification programs and semiconductor device layout programs. Accordingly, a need exists for an alternative approach which significantly simplifies the obtaining of a given logic function from a base array.

SUMMARY

In accordance with this invention, I provide a structure which I denote as a configurable logic array which allows changing the configuration of the finished integrated circuit from time-to-time (even when the integrated circuit is installed in a system) to provide any one of a plurality of logical functions from the same integrated circuit. In accordance with my invention, by providing a number of "configurable logical elements" (also referred to herein as "logic elements") in the base array, a new type of integrated circuit is achieved which is capable of being configured to provide any one of a plurality of logic functions depending upon the tasks which the system of which it is a part is called upon to perform. By "configurable logical element" I mean a combination of devices which are capable of being electrically interconnected by switches operated in response to control bits to form any one of a plurality of logical functions.

A configurable logic array of my invention is comprised of a multiplicity of configurable logic elements each of which can include all the circuit elements necessary to provide one or more of the functions provided by an AND gate, flip flop, inverter, NOR gate, exclusive OR gate, and combinations of these functions to form more complex functions. In accordance with my invention, the particular function to be carried out by a configurable logic element is determined by control signals applied to the configurable logic element from control logic. Depending on the control signals, the configurable logic

element of one embodiment of my invention can function as an AND gate, an OR gate, a NOR gate, a NAND gate or an exclusive OR gate or any one of a number of other logic elements without any change in physical structure. In accordance with my invention, structure is provided to allow any one of a plurality of functions to be selected from each configurable logic element. This is done by providing control logic to store and generate control signals which control the configuration of each configurable logic element.

In one embodiment of my invention, the control signals are stored and transmitted by control logic formed integrally with and as part of the integrated circuit chip containing the configurable logic element. However, if desired the control information can be stored and/or generated outside this integrated circuit and transmitted through pins to the configurable logic element.

In general, in accordance with my invention, a given set of control signals is transmitted to one configurable logic element to control the configuration of that configurable logic element. The control logic is thus arranged to provide any one set of a plurality of sets of control bits to each configurable logic element on the chip. The actual set of control bits provided to each configurable logic element on the integrated circuit chip depends on the function to be carried out by the integrated circuit chip or by each configurable logic element on the chip. The configuration of each logic element on the chip is determined by the intended function of the total chip and by the intended formation of that configurable logic element as part of the chip. Thus the resulting structure is known as a "Configurable Logic Array" or "CLA" and each logic element in the array is known as a "Configurable Logic Element" or "CLE".

In general, each integrated circuit chip has, in addition to and associated with the control logic certain on-chip data routing circuitry. In one embodiment the on-chip data routing is achieved by using a memory to

store the particular data used to configure the configurable logic elements and by then transferring the data from the memory to a novel combination of a dynamic shift register and static latch element within or associated with each configurable logic element on the chip.

The particular structure of this invention is versatile in that it can be implemented particularly easily using P channel, N channel, or CMOS technologies in the embodiment shown. Of course, structure incorporating the principles of this invention can, if desired, be implemented using any other appropriate semiconductor technology. The novel dynamic shift register-static latch element of this invention is particularly useful in that the structural "overhead" (i.e., access circuitry and routing circuitry) is kept to a minimum relative to the useful logic functions on the total chip. Of particular importance, no addressing, data selection, or decoding in each configurable logic element is necessary when this novel combination of a dynamic shift register and static latch element is used to implement the configurable logic array of my invention.

This invention will be more fully understood in conjunction with the following detailed description taken together with the drawings.

Description of the Drawings

Figure 1 illustrates some of the various logic functions capable of being integrated in each logic element in a configurable logic array;

Figure 2 illustrates the internal logic structure of one possible logic element capable of implementing a number of useful functions with two variables A, B and certain configuration control bits, C0 through C5;

Figure 3A illustrates a 16 bit RAM select circuit wherein any one of sixteen possible input states is capable of being identified and 2^{16} functions are capable of being implemented;

Figure 3B illustrates a selection structure for selecting any one of sixteen bits capable of implementing

2^{16} functions, for transmittal to an output lead;

Figure 3C illustrates one possible Karnaugh plot for the structure of Figure 3A;

Figure 3D illustrates the logic gates represented by placing a binary one in the Karnaugh map of Figure 3C at the intersections of the first and second rows and the first column.

Figure 4A illustrates one embodiment of my invention wherein a plurality of configurable logic elements (shown as nine logic elements) are formed on an integrated circuit chip together with programmable interconnects formed between selected leads to yield desired logic functions and with selected input/output pads and interconnections of the leads between logic elements;

Figure 4B shows the key to the cross-connections between crossing conductive leads in Figure 4B;

Figure 5 represents a portion of the circuitry of a novel combination static and dynamic shift register appropriate for use with the configurable logic array of this invention;

Figures 6A through 6H represent wave forms of use in explaining the operation of the novel structure of Figure 5;

Figure 7A represents a schematic diagram of a configurable logic array showing nine of N configurable logic elements where N is a selected integer greater than 9 and selected interconnections between conductive leads;

Figures 7B-1 through 7B-7 are the key showing the types of interconnections made by the symbols shown in Figure 7A;

Figure 8A illustrates a system with a microprocessor controller and four configurable logic arrays;

Figure 8B illustrates a combination of four configurable logic arrays together with a nonvolatile memory;

Figures 9A through 9G illustrate various topologies for forming interconnections between two or more leads on a configurable logic array;

Figures 10A and 10B show the bidirectional circuit of Figures 4A and 4B; and

Figure 11 shows a single board microcomputer using the Configurable Logic Array of this invention.

DETAILED DESCRIPTION

The following detailed decription of this invention is meant to be illustrative only and not limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of the following disclosure.

Turning now to Figure 1, Figure 1 illustrates certain logic functions capable of being integrated into a configurable logic element. The 28 functions shown in Figure 1 are merely illustrative and other elements not shown can, if desired, be included in a configurable logic element. The following elements are shown:

Element	Function
1	AND gate
2	NAND gate
3	AND gate with inverted input
4	NAND gate with inverted input
5	OR gate
6	NOR gate
7	exclusive OR gate
8	exclusive NOR gate
9	3 input AND gate
10	3 input NAND gate
11	3 input OR gate
12	3 input NOR gate
13	OR gate with one input comprising AND gate
14	NOR gate with one input comprising AND gate
15	AND gate with one input comprising OR gate
16	NAND gate with one input comprising OR gate
17	3 input AND gate with one input inverted
18	3 input NAND gate with one inverted input
19	3 input OR gate with one inverted input
20	3 lead NOR gate with one inverted input
21	one of two inputs multiplexer
22	inverting one of two inputs multiplexer

23 "D" flip flop with reset

24 Set-Reset latch

25 "D" flip-flop with reset and inverted output

26 Set-reset latch with reset and inverted output

27 "D" flip-flop with set

28 "D" flip-flop with set and inverted output

Of course, other logic elements can also be implemented in accordance with this invention.

Figure 2 illustrates the internal logic structure of one possible logic element which is capable of implementing all useful functions of the two variables A and B, with the functions being selected by configuration control signals C0, $\bar{C0}$, C1, $\bar{C1}$... through C5, as shown in Figure 1. For example, to implement an AND gate function using the structure shown in Figure 2, the input leads labeled A and B are shunted past inverters 21 and 22, respectively, by high level signals on the C1 and C0 configuration control leads. Leads C1 and C0 are connected to well-known pass transistors 29c and 29d. (Throughout this specification a pass transistor will be represented by the symbol shown within the circles 29c and 29d). Low level signals are applied to the configuration control leads $\bar{C0}$, $\bar{C1}$, C4. Assuming that C0, C1 and all of the other leads are connected to N channel MOS pass transistors, the control signals, C2, $\bar{C2}$, C3 and $\bar{C3}$ are "don't cares". That is, these signals can be high or low without affecting the output signal. In addition, a high level signal on C5 is applied to enable AND gate 25. The high level signal from AND gate 25 is passed through NOR gate 26. From NOR gate 26 this signal proceeds as a low level signal to turn off MOS transistor 29a (the source of which is grounded and the drain of which is connected to the output lead 28) and to turn on through NOR gate 27 N channel transistor 29b (the drain of which is connected to a power supply and the source of which is connected to

both the output lead 28 and the drain of N channel transistor 29a). Thus the structure of Figure 2 configured as described above is an AND gate. Other logic functions can also be produced by appropriate selection of the control signals to be supplied to the configuration control leads C0 through C5 to activate the appropriate pass transistors and gates within the structure.

Figure 3A illustrates a 16 bit RAM capable of to producing an output signal in response to any one of sixteen possible combinations of input signals. Thus input signals A and B control the X decoder to select any one of the four columns in the 16 bit RAM. Input signals C and D control the Y decoder to select any one of the four rows in the 16 bit RAM. The 16 bit RAM produces an output signal representative of the bit at the intersection of the selected row and column. There are 16 such intersections and thus sixteen such bits. There are 2^{16} possible combinations of functions capable of being represented by 16 bits. Thus, if a NOR gate is to be simulated by the 16 bits in the RAM, the Karnough map for the RAM would be as shown in Figure 3C. In Figure 3C all bits are "0" except the bit at the intersection of the first row (representing A=0, B=0) and the first column (representing C=0, D=0). Should a less frequently used function be desired to be generated by the 16 bit RAM, (for example, should a "1" output signal be desired for A=1, B=0, C=0 and D=0) then a binary "1" is stored at the intersection of the second row and the first column. Should a binary "1" be desired both when A=0, B=0, C=0 and D=0 and also when A=1, B=0, C=0 and D=0, then a binary "1" is stored at each of the intersections of the first column with the first row and the second row. The logic circuit represented by this loading of the RAM is as shown in Figure 3D. Thus the RAM of Figure 3A represents an elegant and simple implementation of any one of 2^{16} logic functions.

Figure 3B shows another structure for yielding any one of sixteen select bits. Each of registers 0-15 in

the vertical column to the left labelled "16 Select Bits", contains a selected signal, either a binary 1 or 0. By selecting the proper combination of A, B, C, and D, a particular bit stored in a particular one of the sixteen locations in the 16 Select Bits register is transmitted to the output lead. Thus, for example, to transmit the bit in the "1" register to the output lead, the signal A, B, C, D is applied to the leads so labeled. To transmit the signal labeled "15" in the sixteenth location in the 16 Select Bits register to the output lead, the signal A, $\bar{B}$, $\bar{C}$, and $\bar{D}$ is applied to the appropriate columns. Again, any one of 2^{16} logic functions can be implemented using this structure.

Figures 4A illustrates an embodiment of a of a configurable logic array of this invention containing nine configurable logical elements. As shown in Figure 4A, nine logical elements are placed on an integrated circuit chip together with interconnects and variable switches for connecting various leads to other leads. Each of logic elements 40-1 through 40-9 represents a collection of circuitry such as that shown in Figure 2 or some similar structure capable of being configured as described above in Figure 2 to perform any one of a number of logic functions. To program the circuitry, selected signals are applied to input leads identified as configuration control input leads thereby to generate a desired logical function in each of the logic elements. In Figure 4A, no specific lead has been identified as an input lead for the configuration control signals. However, any particular I/O pad can be selected for this purpose. The configuration control bids can be input into the configurable logic array either in series or in parallel depending upon design considerations. In addition, another I/O pad will be used on input clock signals to clock the logic elements both for the shifting in of the configuration control signals to each configurable logic element and for controlling the operation of each logic element during the functioning of the integrated circuit chip in its intended

manner. The combination of logic elements 40-1 through 40-9 yields the desired logical output for the Configurable Logic Array. Figure 4B illustrates the meaning of the interconnect symbols used in Figure 4A.

To configure a logic element such as logic element 40-1 (Figure 4A, 4B) a number of bits must be applied to the configuration control leads such as leads C0 through C5, as shown, for example, in Figure 2. To do this, a shift register is utilized, in the preferred embodiment, as part of each configurable logic element. Figure 5 illustrates a novel shift register of use in this invention. The shift register of Figure 5 is illustrated showing two basic storage cells. Each storage cell is capable of storing one bit of information. Of course, an actual shift register will contain as many storage cells as required to configure the logic element of which the shift register is a part, to its desired configuration. In operation, an input signal is applied to input lead 58. This input signal (shown in Figure 6D) contains the pulses to be stored in the shift register as configuration control bits to configure the configurable logic element to perform a desired logic function or to configure an interconnection between leads in a manner to be described shortly. Thus the sequence of pulses applied to input lead 58 represents those pulses which when stored in the storage cells of the shift register will activate the configuration control bits in the proper manner to achieve the desired functional and/or interconnection result. For example, if the circuit of Figure 2 is to be configured to form an AND gate, the pulses C0, C1, C2, C3, C4, and C5 would be represented by 1,1,X,X, 0,1.

The sequence of pulses applied to input lead 58 is synchronized with clocking pulses $\phi 1$ and $\phi 2$ applied to leads 57 and 59 respectively. Thus in the first period of operation clocking pulse $\phi 1$ goes high (Fig. 6A), clocking pulse $\phi 2$ is low (Fig. 6B), the hold signal (Fig. 6C) is low during shifting thereby facilitating the

passage of data through sequentially connected cells 5-1, 5-2 et al. of the shift register. To shift the pattern 01010 into the shift register, the following operations occur: The input signal on lead 58 is low during approximately the first half cycle of the clocking period t1. The output signal $\bar{Q}\bar{1}$ of inverter 51-1 goes to a high level in response to the low level input signal and $\Phi 1$ high to enable PASS transistor 53-1. Come time through the first clocking period t1, the clock signal $\Phi 1$ goes low (Fig. 6A) and the clock signal $\Phi 2$ shortly thereafter goes high (Fig. 6B) to enable PASS transistor 55-1. Consequently, the high level output signal $\bar{Q}\bar{1}$ is transmitted to the input lead of inverter 52-1 by enabled pass transistor 55-1 and thereby produces a low level output signal Q1 on the output lead of inverter 52-1. Thus at the end of period t1, the output signal Q1 (Figure 6F) from inverter 52-1 is low level. The output signals $\bar{Q}\bar{2}$ and Q2 from inverters 51-2 and 52-2 in the second cell are still indeterminate because no known signal has yet propagated to the second storage cell 5-2 to change the signals of these inverters to a known state.

At the beginning of the second period (labeled "t2" in Fig. 6A), $\Phi 1$ goes high (Fig. 6A) and $\Phi 2$ is low (Fig. 6B) having gone low before period t1 ended. The input signal (Figure 6D) now has risen to a high level representing a binary 1 and thus the output signal $\bar{Q}\bar{1}$ of inverter 51-1 has gone low. The output signal Q1 of inverter 52-1 remains low because pass transistor 55-1 is held off by the low level $\Phi 2$ signal. Some time through the second period $\Phi 1$ goes low followed a fraction of time later by $\Phi 2$ going high. At this time, the output signal $\bar{Q}\bar{1}$ is transmitted through pass transistor 55-1 to inverter 52-1 thereby driving the output signal Q1 from inverter 52-1 to high level. Meanwhile, during period t2 the previous low level signal on Q1 has driven the output signal $\bar{Q}\bar{2}$ of inverter 51-2 to a high level when Q1 was at a high level to enable PASS transistor 53-2 and the change in $\Phi 2$ from a low level to a high level in the

second half of period t2 to enable PASS transistor 55-2 drives the output signal Q2 from inverter 52-2 to a low level. In this manner, the input signal on lead 58 (Fig. 6D) is transmitted through each of the cells 5-1, 5-2, 5-3 et al. in the shift register. Upon the transfer into the shift register of the desired information, the hold signal (Figure 6C) is enabled (i.e., driven to a high level) thereby to connect the feedback leads 50-1, 50-2, and 50-3 et al. from the output leads of inverters 52 to the input leads of inverters 51 so as to hold the information then in each cell indefinitely. In operation, the signal stored in a given cell 5 is connected to a configuration control or to an interconnect pass device.

The $\bar{Q}_1$, Q_1, $\bar{Q}_1$, Q_2, etc., of the shift register are directly connected to the (configuration) control inputs of a logic unit or the pass devices of the configurable interconnect.

When $\Phi 1$ is low, $\Phi 2$ and hold may be brought high, thus holding the data indefinitely. The entire shift register may be set or cleared by setting or clearing the input with $\Phi 1$ and $\Phi 2$ both high and HOLD low. Enough set/reset time must be allowed for the signal to propagate the entire length of the shift register to clear the shift register in this manner. Naturally this time is dependent upon the length of the shift register.

The shift register operates in its dynamic phase by storing the information being shifted as charge on the gates of the transistors (not shown in Figure 5 but well-known) comprising inventers 51-1, 52-1, 51-2, 52-2 et al. of the shift register. These inverters are of well-known design and will not be described in detail. The use of dynamic shift register is an important feature of the invention because a dynamic shift register uses six transistors and thus takes up very little area. Uniquely, the dynamic shift register is converted to a static latch by adding only one transistor. Thus the novel dynamic shift register-static latch can be easily fabricated as part of a configurable logic element without adding significant complexity to the circuit or consuming

significant semiconductor area. Because of the "hold" signal, the dynamic shift register can be driven at a very low frequency because placing the shift register on hold automatically refreshes the data. Thus a separate refresh circuit is not needed.

It will be apparent from the above description that the novel, dynamic shift register static latch circuit is unique in that it does not need refreshing once it has been latched into a hold position. This is accomplished by use of the feedback circuit comprising lead 50-1 and pass transistor 54-1 in cell 5-1, for example.

Figure 7A shows an additional configurable logic array containing a plurality of configurable logic elements. In particular, configurable logic elements 70-1, 70-2, 70-4 and 70-5 are shown in their entirety while configurable logic elements 70-3, 70-6 and 70-7 through 70-9 are shown partially. In particular, the complete interconnections of these last five logical elements are not shown. The structure shown in Figure 7A is merely illustrative of the types of configurations and connections which can be implemented using the configurable logic array of this invention and does not depict an actual circuit configured to carry out an intended function.

As shown in Figure 7A, given leads can be interconnected by any one of a plurality of different means (i.e., interconnection structures). The symbols representing the interconnections shown in Figure 7A are illustrated in Figure 7B. In particular, while the schematics depicting various interconnections are to some extent self-explanatory, the conventions used in these schematics are explained in Figures 9A through 9G.

Figure 9A is the schematic of a circuit for making a number of different interconnections between two cross-over leads, horizontal lead 90-1 and vertical lead 90-2. Thus, in Figure 9A pass transistor 2, when activated into the conducting state, connects lead 90-3 to lead 90-1. Pass transistor 1, when conducting, connects lead 90-3 to

lead 90-4. Pass transistor 4, when conducting, connects lead 90-4 to lead 90-2 and pass transistor 3, when conducting, connects lead 90-1 to lead 90-2. Pass transistors 5 and 6, when off, separate leads 90-2 from lead 90-3 and separate lead 90-1 from lead 90-4 respectively. Thus, should it be desired to connect vertical lead 90-2 to vertical lead 90-3, pass transistor 6 is activated. Likewise, should it he desired to connect horizontal lead 90-1 to horizontal lead 90-4, pass transistor 5 is activated. The terminology used to represent the possible connections between a plurality of leads can become quite complex. Thus, a simplified notation system as shown in Figures 9B to 9E has been adopted.

In Figure 9B, a plurality of pass transistors 92-1 through 92-13 are shown. The convention adopted in Figure 9B is to have a given pass transistor represented by a single short line. Thus, the line labelled 92-1 represents a pass transistor. Pass transitor 92-1 is drawn so that its two ends point to the ends of the leads 91-5 and 91-6 being interconnected by pass transistor 92-1. Thus, the right end 93a of pass transistor 92-1 is aimed to the end 94a of lead 91-5. The left end 93b of pass transistor 92-1 is aimed to the end 94b of lead 91-6. For simplicity and to avoid cluttering the drawing in Figure 9B, the other ends of the transistors are not labelled. However, by visually aligning the line representing a given pass transistor with the ends of the leads 91-1 through 91-6 the particular two leads interconnected by that pass transistor can be determined. Thus, pass transistor 92-7 interconnects horizontal lead 91-4 with horizontal lead 91-1. Pass transistor 92-13 interconnects horizontal lead 91-4 with horizontal lead 91-2. Pass transistor 92-12 interconnects lead 91-3 with lead 91-5. Similar connections can be made between the other pass transistors and the other leads.

The above description assumes that only two leads are to be interconnected. If more than two leads are to

be interconnected, the structure of Figure 9B can also be used for this purpose. Thus, lead 91-3 can be connected by turning on pass transistor 92-10 to lead 91-2. Simultaneously, lead 91-3 can be connected to lead 91-4 by turning on pass transistor 92-13. Alternatively, lead 91-3 could be connected to lead 91-4 by turning on pass transistor 92-11. Of course, this would also connect lead 91-4 through lead 91-3 and pass transistor 92-10 to lead 91-2. In addition, lead 91-6, for example, could be connected to the three leads 91-2, 91-3, 91-4 by turning on pass transistor 92-8. The number of interconnections which can be made using this structure is limited only by the imagination of the designer. In the limit, if all the pass transistors are turned on, all the leads 91-1 to 91-6 are interconnected. The resulting structure has a large capacitance which can actually be used in circuits as a component. Of course, all leads in Figure 9B can be interconnected by turning on as few as five leads. Note that in Figure 9B leads 91-1 and 91-2 cannot be directly connected to each other nor can lead 91-4 be directly connected to lead 91-5 without involving another lead. However, this ommission is not of importance because in an integrated circuit there is no need for two horizontal leads to carry the same signal in general. Of course, two additional pass transistors could be added to the structure of Figure 9B if Figure 9B is considered to be merely a symbolic representation of intersecting leads and leads 91-1 and 91-2 are merely shown for convenience as being parallel but in fact represent non-parallel leads on an integrated circuit.

Turning to Figure 9D another possible interconnection topology is illustrated. In Figure 9D leads 1 to 8 are shown coming together at a complicated intersection. Leads 1 and 8 are parallel horizontal to the left, leads 4 and 5 are parallel horizontal to the right, leads 2 and 3 are parallel vertical up and leads 6 and 7 are parallel vertical down. Looking for a moment at lead 6, the end

6a of lead 6 can be connected sensibly to the ends "a" of leads 1, 2, 3 , 4, 5 and 8. It is not sensible to connect lead 6 to lead 7 because theoretically the two leads are going in one direction only one lead is required to carry the necessary information in that direction. Since lead 6 has six possible connections and there are eight leads, a total of forty-eight possible connections are offered by the structure of Figure 9D. Since a given pass transistor connects two ends, twenty-four pass transistors are required to make the required forty-eight connections. The particular pass transistors have their ends labelled in Figure 9-D to illustrate the leads which are connected by a given pass transistor. Thus, pass transistor 6-8 interconnects the end 6a of lead 6 to the end 8a of lead 8. Pass transistor 7-5 interconnects the end 7a of lead 7 to the end 5a of lead 5. Because of the complexity of the structure of Figure 9D a slightly different convention (a line with numbers on both ends) has been adopted for representing the pass transistor than was described above in conjunction with Figure 9B.

Figure 9E illustrates types of interconnections possible using the method of this invention. The leads interconnected are illustrated by showing continuous lines or broken lines depending on whether a given lead is connected to another lead or left unconnected. These interconnections are self-explanatory.

Figure 9F illustrates the connections that would be possible if the four pass transistors omitted from Figure 9D were in fact included. The dashed lines show the interconnections possible by these omitted transistors. Thus, Figure 9D shows only twenty pass transistors whereas twenty-four pass transistors are necessary to make all possible nonsimple connections. Figure 9G illustrates, however, the way in which it is possible to interconnect leads 4 and 7 without the four transistor connections shown in Figure 9F being present. Thus, to connect lead 4 to lead 7, lead 4 is connected directly to lead 8 by

means of transistor 4-8 while lead 8 is connected to lead 7 by pass transistor 8-7.

Figure 9C illustrates the configuration of Figure 9D with the full twenty-four interconnection transistors shown rather than merely the twenty shown in Figure 9D. As shown in Figure 9C pass transistors 1-6, 7-4, 2-5 and 8-3 have been added to the transistors shown in Figure 9D. For convenience and to avoid cluttering the drawing, the other pass transistors shown in Figure 9D have not been numbered in Figure 9C except for pass transistor 6-8.

Note that each of the interconnections shown above in Figures 9A through 9G requires only one gate in order to connect one lead to another except for the particular configuration illustrated in Figure 9G wherein two gates are required. This means that the speed of circuits formed using the interconnections of this invention is greater than the speed of circuits using prior art interconnections.

The symbology used Figures 7B-1 through 7B-7 is identical to the symbology just explained in conjunction with Figures 9A through 9G. Thus, for example, Figure 7B-2 illustrates a solid block involving a twenty pass transistor interchange. This particular twenty transistor interchange is shown in more detail in Figure 7B-7 and corresponds precisely to the interchange explained above in conjunction with Figure 9D.

For convenience, Figure 7B-1 illustrates three transistors capable of making a T connection or a cross-connection but not a full interconnection. By full interconnection is meant the ability to connect each of the leads (in Figure 7B-1, four leads) coming into a node to a given node or to each of the other leads coming into the node in any combination.

Figure 7B-2 shows a one transistor interconnection to connect a row with a column. Figure 7B-3 shows a six transistor full cross interconnection wherein any one of

four leads coming into a node can be connected to any one of the other three leads. Figure 7B-4 shows six leads coming into an intersection wherein ten pass transistors are used to interconnect any one of the six input leads to any one of the five other leads input to the node. Figure 7B-5 illustrates a four-lead node where two horizontal continuous leads are interconnected with two separate vertical leads using five pass transistors.

Figure 7B-6 illustrates a three-transistor interconnection wherein any one of three leads coming into a node can be interconnected with any one of the other two leads. Figure 7B-7 illustrates the twenty-transistor interchange for interconnecting any one of eight input leads to any one of the other eight input leads except that lead parallel and adjacent to the lead being interconnected as illustrated in Figure 9D and except for the four interconnections shown in Figure 9F (which also cannot be directly made using the structure of Figure 7B-7).

Figures 8A and 8B illustrate two possible systems capable of using the configurable logic arrays of this invention. In Figure 8A, a microprocessor microcontroller produces address signals, control signals and data signals which are transmitted to a master configurable logic array. Also shown as N slave CLAs. As shown in Figure 8A, the control bits to control each of the configurable logic elements in each slave configurable logic array are transmitted on the data leads from the microcontroller to the master configurable logic array. From the master configurable logic array, this data is transmitted in series to each one of N configurable logic arrays where N is a selected integer. The control bits for controlling the configuration of each configurable logic element in each of the configurable logic arrays are transmitted in series through slave configurable logic array 1, slave configurable logic array 2 through to the Nth configurable array. The data is stored in serial shift registers as

described above in conjunction with Figure 5. When the proper bits are located in the proper storage cells in each shift register, the hold signal shown in Figure 6C is raised to a high level thereby locking each data bit into the proper location in the corresponding shift register and thus configuring each configurable logic element in each configurable logic array. The data clock signals are applied on a separate lead to each configurable logic array as shown to clock in the control data.

The address arrow pointing to CLA (master) in Figure 8A merely indicates that the microprocessor has the ability to select a particular master configurable logic array for receipt of data from the microprocessor. In Figure 8B the master configurable logic array is capable going into the nonvolatile memory with addresses to select particular data to be retrieved from the memory to be used to configure each of the salve configurable logic arrays. In Figure 8A the microprocessor produces address signals which will go to off chip memory or to other circuitry (not shown).

In Figure 8B the structure is similar to that shown in Figure 8A except that a nonvolatile memory such as a ROM, EPROM or E^2PROM is used as the source for the configuration control bits to be transmitted into each of the configurable logic arrays. The structure of Figure 8B is unique in that when power is turned on or when a reset signal is applied to the master CLA, the master CLA initiates the transfer of the information for controlling the transfer of the information for controlling or configuring the Configurable Logic Array from the non-volatile memory to the master CLS and to the slave CLAs 1to N. In this sense, the structure of Figure 8B is self-configuring in response to power on or a reset signal.

A single board microcomputer using a Configurable Logic Array of this invention is shown in Figure 11. Configurable Logic Array 110 performs the chip decode

functions, the latching functions and the various special logic that is necessary to implement a single board microcomputer. The CLA has an output lead ("DONE") which is low from the time the power is turned on until the single board microcomputer is fully functional.

The first event that occurs when power is turned on is that the Configurable Logic Array 110 forces the Z8000 CPU 111 into the reset state. Reset forces the outputs of the CPU to be tri-stated (i.e., to go to high impedance level) which makes it possible for the Configurable Logic Array to use the control lines from the CPU 111 while it is being configured. The Configurable Logic Array 110 through a set of address lines (LA_1 - LA_{12}) addresses the EPROMS which are also used for the bootstrap of the microprocessor. In addition, the EPROMS have available in them configuration information for the CLA 110. The CLA 110 has signals which, during the self-loading time, are fixed high, fixed low so that particular bi-directional buffers 112 can be set in the correct direction for loading data from the EPROMS 113 to the Configurable Logic Array 110. Configurable Logic Array 110 then sequentially addresses locations in the EPROMS 113 which are read into the Configurable Logic Array 110 to configure the CLA 110. When array 110 is totally configured it then takes on its new functions and unlatches the done output which releases the reset line to the CPU 111. CPU 111 is then in control of the entire system. The decode used herein decodes the addresses from the CPU to create chip enables and chip selects for the various RAMS and EPROMS in the system and for the I/O devices as well.

The bi-directional selectable buffer shown in Figures 4A and 4B is illustrated in more detail in Figures 10A and 10B. Figure 10A shows the bi-directional buffer as comprising an inverter 101 connected into a second CMOS inverter comprising p-channel transistor 103 and n-channel transistor 104, the output lead of which is gated by pass transistor 108. In the other direction, inverter 102

feeds an input signal onto the gates of p-channel pass transistor 105 connected in series with n-channel transistor 106. The output at the node between the p- and n-channel transistors is controlled by pass transistor 107. The pass transistors 107 and 108 are activated by the Q, $\bar{Q}$ signals from the storage element which can comprise a standard flip-flop. Thus, the buffer passes a signal in one direction or the other on leads 109a or 109b, depending upon whether or not pass transistor 107 or pass transistor 108 is turned on.

Figure 10B illustrates schematically the circuit of Figure 10A. In Figure 10B, the series connected p-channel and n-channel transistors 103 and 104 have been represented by inverter 103' and series connected p-channel pass transistor 105 and n-channel pass transistor 106 have been represented by inverter 105'. Of course, in operation, the two circuits are identical.

In Figure 4A directional amplifiers (shown by an X in a box) are used to amplify signals which have been attenuated by a number of pass transistors. This speeds up considerably the operation of the circuit. The delay of a signal increases approximately in proportion to the square of the number of pass transistors through which a signal must pass. The amplifer brings the signal voltage back to its normal level.

In view of the above description, it will be obvious to those skilled in the art that a configurable logic element in a Configurable Logic Array is capable of being reconfigured even after the Configurable Logic Array has been installed in a circuit. Indeed, this is one of the key advantages of the Configurable Logic Array of this invention. Thus, a configurable Logic Array can be reconfigured to provide a new logical function as part of its normal operation in the system of which it is a part.

Another advantage of this invention is that the I/O pads can be used as either input or output pads and can connect to any internal signal using pass transistors.

While one embodiment of this invention has been described, other embodiments of this invention will be obvious in view of the above disclosure.

The figures used in the claims are only meant to explain more clearly the intention of the invention and are not supposed to be any restriction concerning the interpretation of the invention.

I claim:

1. A shift register comprising:

a plurality of dynamic storage cells 1 through K connected in series where K is a selected integer representing the maximum number of storage cells in series;

means for transferring data sequentially from one cell to the next cell so as to fill all the cells of the shift register; and

means for holding the data in each cell indefinitely.

2. Structure as in Claim 1 including:

means for generating from the data in said plurality of storage cells a corresponding plurality of configuration control bits to be used for controlling the configuration of a configurable logic element.

3. Structure as in Claim 1 wherein each of said storage cells comprises

a first inverter possessing a first input lead and a first output lead, said first input lead having a first capacitance associated therewith;

a second inverter possessing a second input lead and a second output lead, said second input lead having a second capacitance associated therewith;

a first pass transistor connected between the output lead of said first inverter and the input lead of said second inverter;

a second pass transistor connected between the output lead of said second inverter and the input lead of said first inverter, thereby to form a feedback path from said output lead of said second inverter to the input lead of the first inverter;

means for turning on and off said first transistor;

means for turning on and off said second transistor,

wherein when said first and second pass transistors are turned on said first inverter and said second inverter are latched to maintain a given state.

4. Structure as in Claim 3 wherein said means for turning on and off said first transistor comprises a source of a clocking signal and said means for turning on and off said second transistor comprises a hold signal for latching up said first and said second inverter.

5. Structure as in Claim 4 including means for gating information in series from an external source into the first of said plurality of storage cells.

6. Structure as in Claim 1 wherein each cell holds a selected bit and its complement.

7. Structure as in Claim 3 wherein the data being transferred from one cell to the next is stored between transfer as a charge on said first capacitance and said second capacitance.

8. Structure comprising

an integrated circuit comprising a plurality of logic elements, each of said logic elements composed of a number of semiconductor devices and being capable of being configured to perform any one of a plurality of logic functions; and

means for configuring each of said logic elements to perform a selected one of said plurality of logic functions.

9. Structure as in Claim 8 wherein said semiconductor devices in each of said logic elements include a plurality of switches, said switches being capable of being activated by electrical signals to configure said semiconductor devices so as to perform a selected one of a set of logic functions.

10. Structure as in Claim 9 wherein said switches comprise pass transistors containing gates and said electrical signals comprise control signals to be applied to said gates.

11. Structure as in Claim 10 wherein each of said logic elements includes means for holding a plurality of control signals, said control signals controlling the states of the electronic switches in said logic element thereby to control the particular logic function carried out by said logic element.

12. Structure as in Claim 11 wherein each of said logic elements includes means for changing the control information contained in said logic element thereby to reconfigure the logic element to carry out another one of said set of functions.

13. Structure comprising a plurality of logic elements contained on a selected integrated circuit, each of said logic elements being interconnected by leads and switching elements thereby to form a configurable logic array.

14. Structure as in Claim 13 wherein said configurable logic array includes

means for changing the state of each of the switches interconnecting said logic elements thereby to configure the configurable logic array to carry out any one of a plurality of logic functions.

15. A system comprising

structure capable of being configured to perform any one of a multiplicity of logic functions;

means for storing information capable of controlling said structure capable of being configured; and

means for transferring said information capable of controlling said structure capable of being configured from said means for storing to said structure capable of being configured.

16. Structure as in Claim 15 wherein said system is formed on a single monolithic integrated circuit.

17. Structure comprising

a plurality of leads; and

means for interconnecting any one of said plurality of leads to any other of said plurality of leads.

18. Structure as in Claim 17 wherein said means for interconnecting any one of said plurality of leads to any other of said plurality of leads includes means for interconnecting any combination of said plurality of leads.

19. Structure as in Claim 18 wherein said means for interconnecting any combination of said plurality of leads comprises

a multiplicity of pass transistors each of said pass transistors being arranged to interconnect one of said plurality of leads to another of said plurality of leads when said pass transistor is turned on.

20. Structure comprising N leads where N is a selected integer, each of said N leads not being connected to the others of said N leads;

M pass transistors, where M is the number of pass transistors required to connect each one of said N leads to any one of the other of said N leads; and

means for activating each of said M pass transistors thereby to form a conductive path from one of said N leads to another of said N leads.

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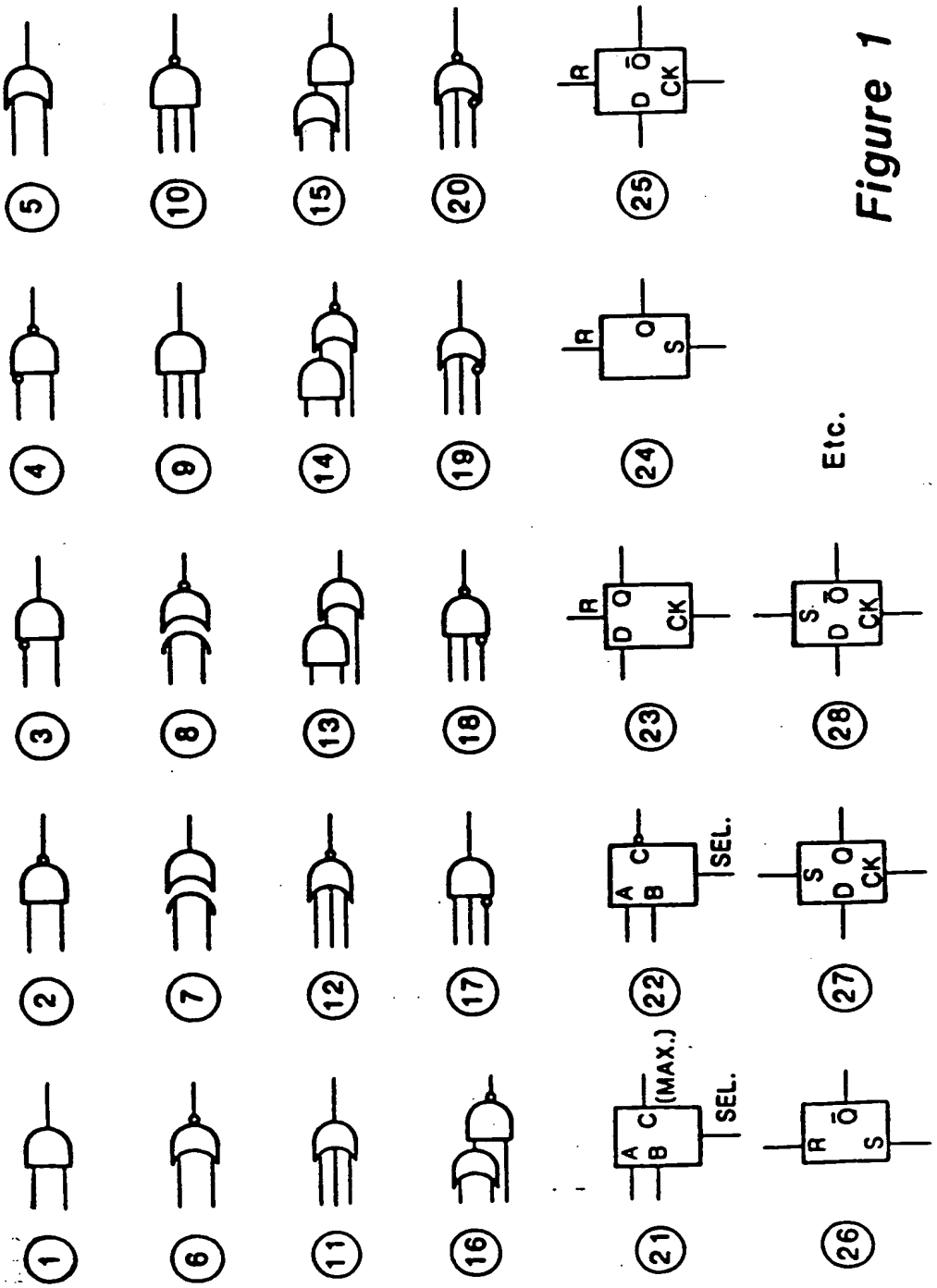


Figure 1

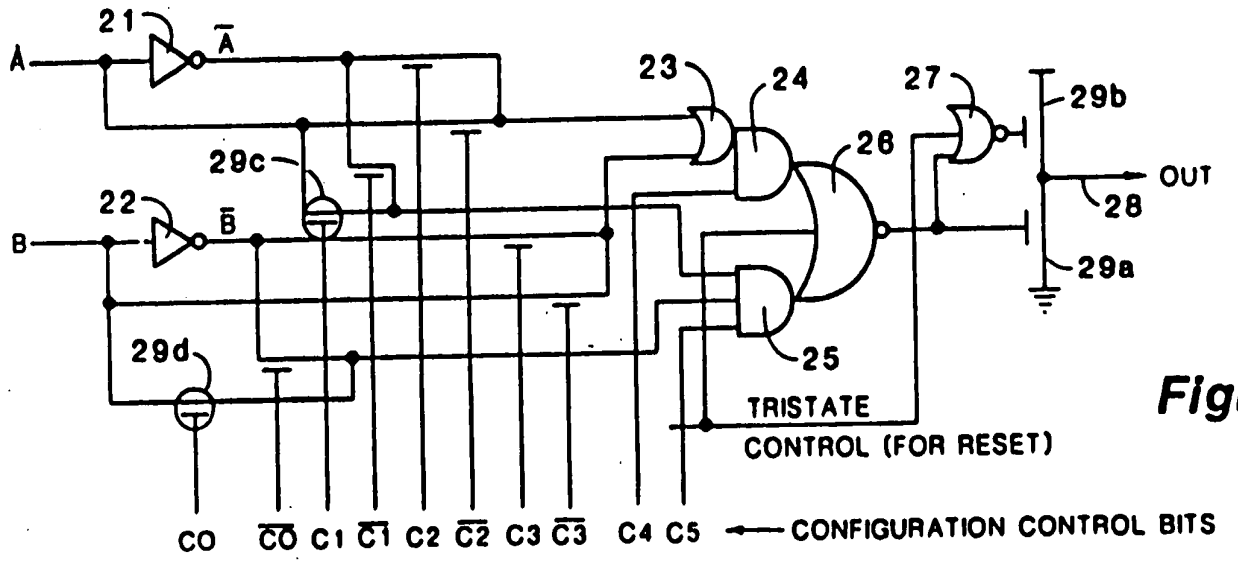


Figure 2

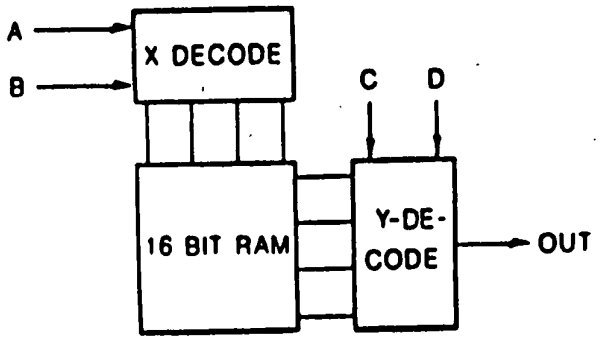


Figure 3A

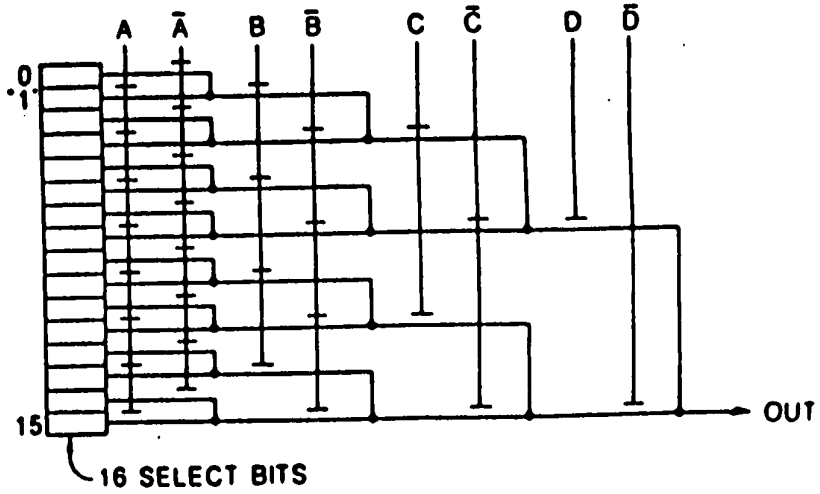


Figure 3B

"2/15"

0204034

A B \ C D	0 0	1 0	0 1	1 1
0 0	1	0	0	0
1 0	0	0	0	0
0 1	0	0	0	0
1 1	0	0	0	0

Figure 3C

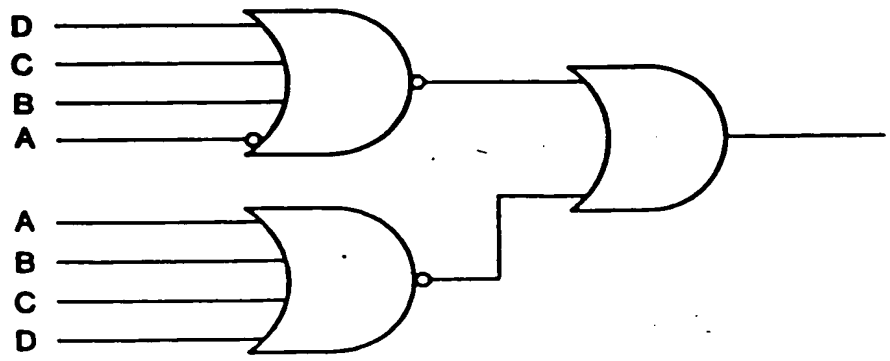


Figure 3D

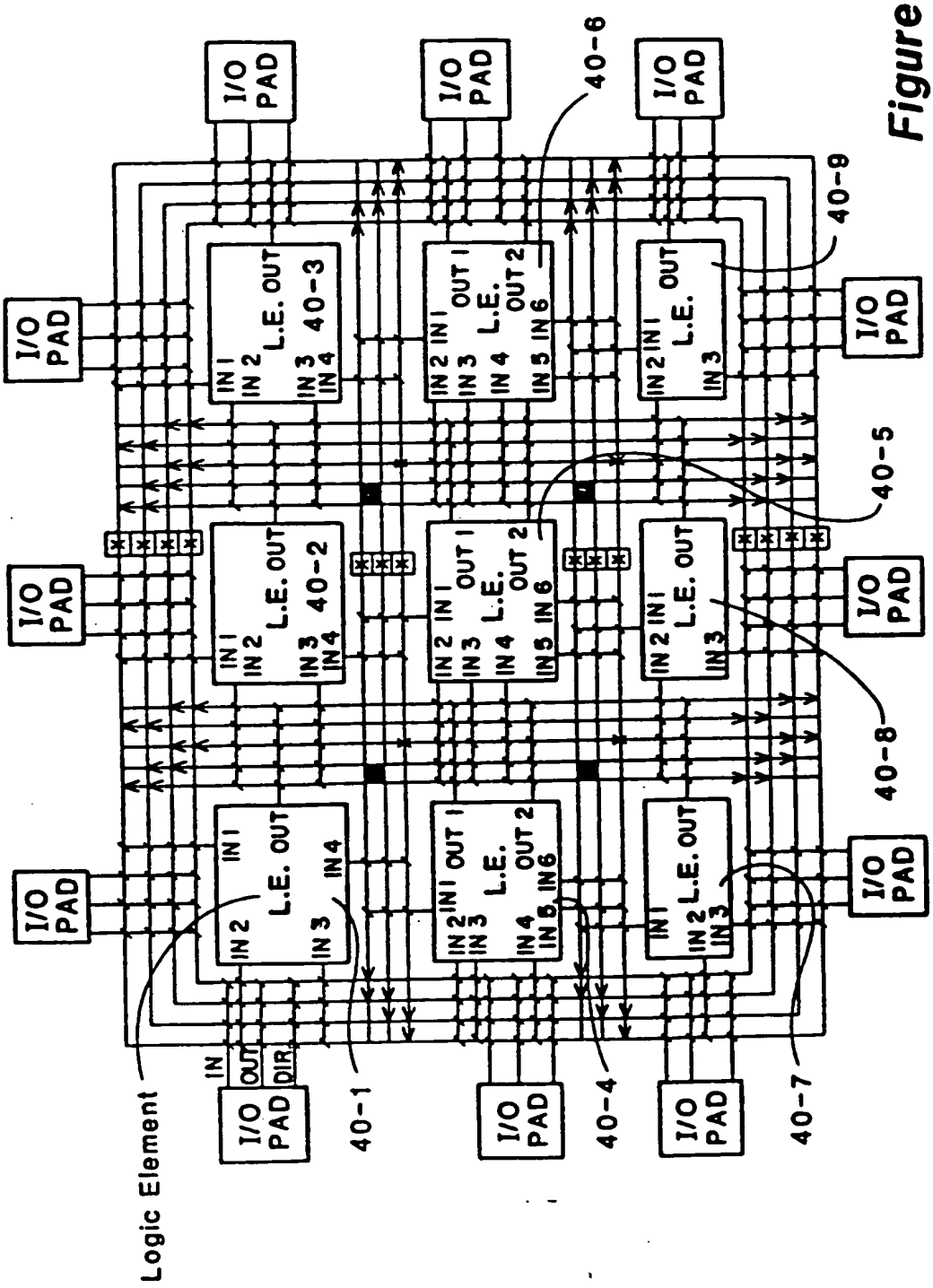
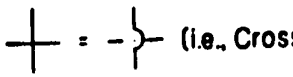

Example of a 3x3 Logic Element CLA with 12 I/O pads & 3 types of L. E.'s
I/O PAD
L.E. OUT
IN 1
IN 2
IN 3
IN 4
IN 5
IN 6
OUT 1
OUT 2
40-1
40-2
40-3
40-4
40-5
40-6
40-7
40-8
40-9
Logic Element
IN
OUT
DIR

Figure 4A

 = (i.e., Crossover without Connection or Possibility of Connection)

 = or (i.e., Can Only be Connected or Disconnected, As Input or Output, But Cannot be Broken)

 = Full Interchange - e.g. Figure 7B-7

 = Full Interchange - e.g. Figure 7B-3

 = Partial Interchange: 

Lines (4 Vertical Shown) that do not have  or  Intersections are Intended to be Low Skew (i.e., Clock or Other) Paths.

 = Directional Amplifier (Direction is Selectable) to Prevent Signal Drooping Through too Many Pass Devices. (Figure 10B)

Figure 4B

"5/15"

0204034

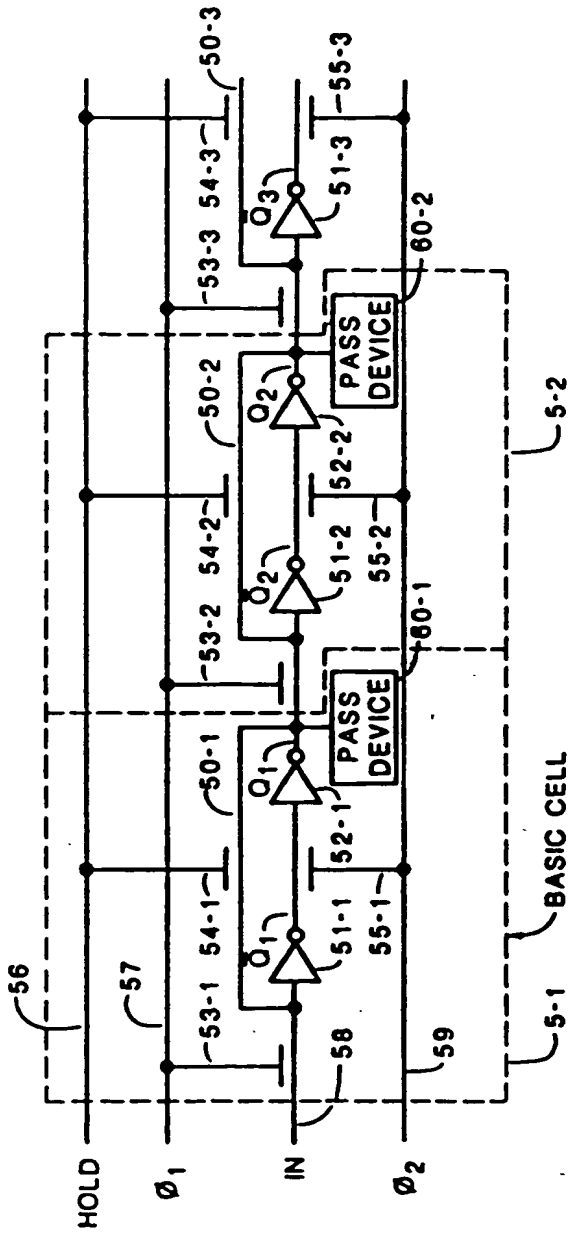
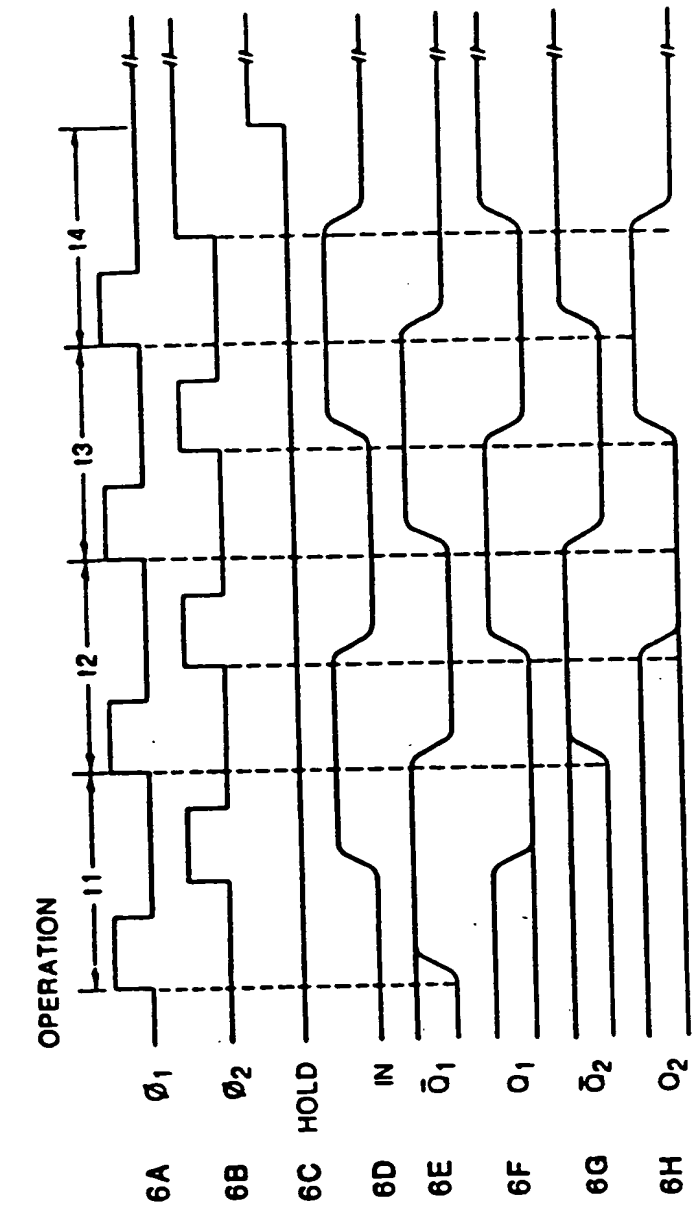

HOLD
Ø1
IN
Ø2
56
57
58
59
53-1
54-1
50-1
51-1
55-1
52-1
PASS DEVICE
60-1
53-2
54-2
50-2
51-2
55-2
52-2
PASS DEVICE
60-2
53-3
54-3
50-3
51-3
55-3
BASIC CELL
5-1
5-2

Figure 5



Timing Diagram Shows 0/0/0 being Shifted into the Shift Register. When ϕ_1 is Low, ϕ_2 and HOLD may be Brought High, thus Holding the Data Indefinitely. The Entire Shift Register may be Set or Cleared by Setting or Clearing the Input with ϕ_1 and ϕ_2 High and Hold Low. Enough Set/Reset Time must be Allowed for the Signal to Propagate the Entire Length of the Shift Register.

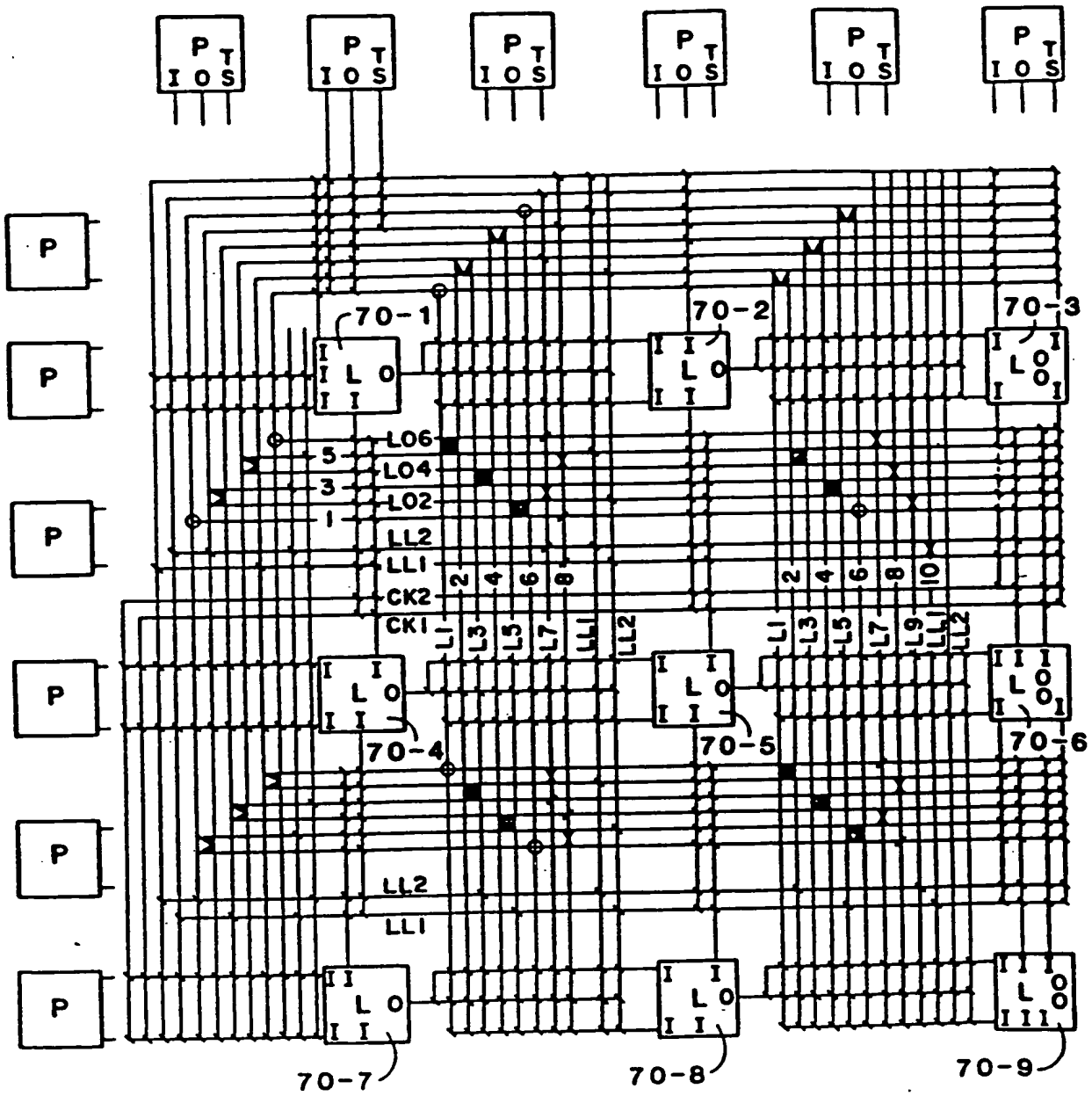

P
I O S
70-1
70-2
70-3
70-4
70-5
70-6
70-7
70-8
70-9
LO6
LO4
LO2
LL2
LL1
CK2
CK1
LL2
LL1

Figure 7A

7B-1 = OR OR OR OR = 3 T =

7B-2 = OR = 1 T

7B-3 = 6 T's FULL CROSS =

7B-4 = 10 T =

7B-5 = 5 T =

7B-6 = 3 T =

7B-7 = 20 T =

Figure 7B

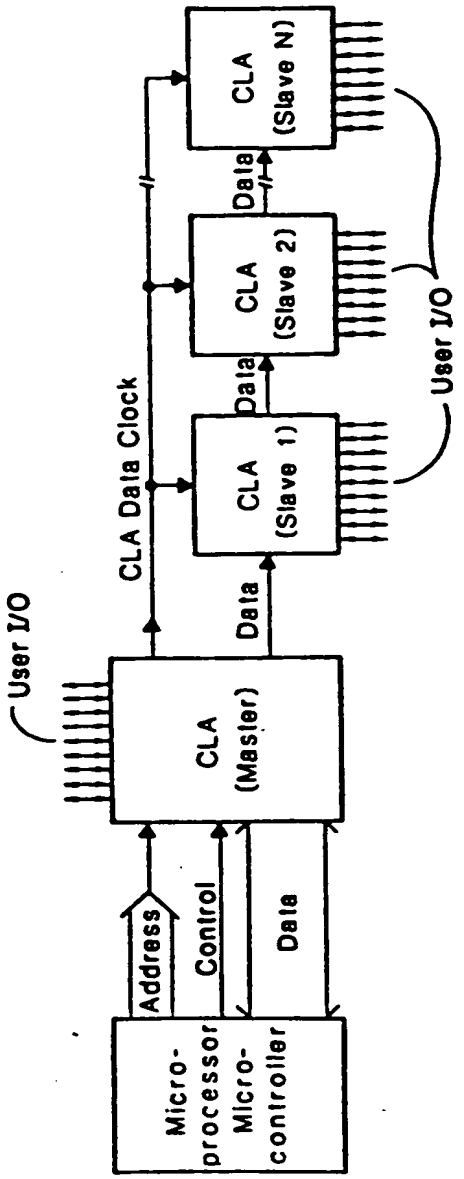


Figure 8A

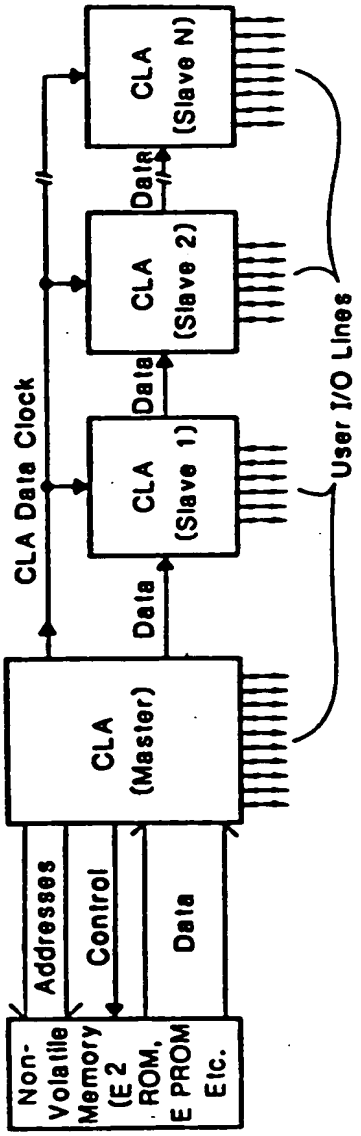


Figure 8B

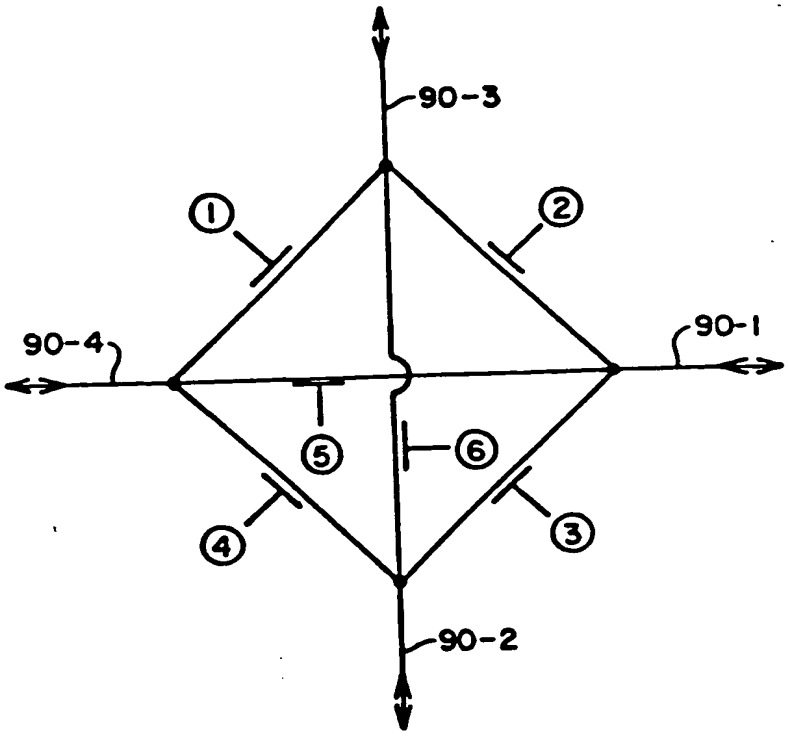


Figure 9A

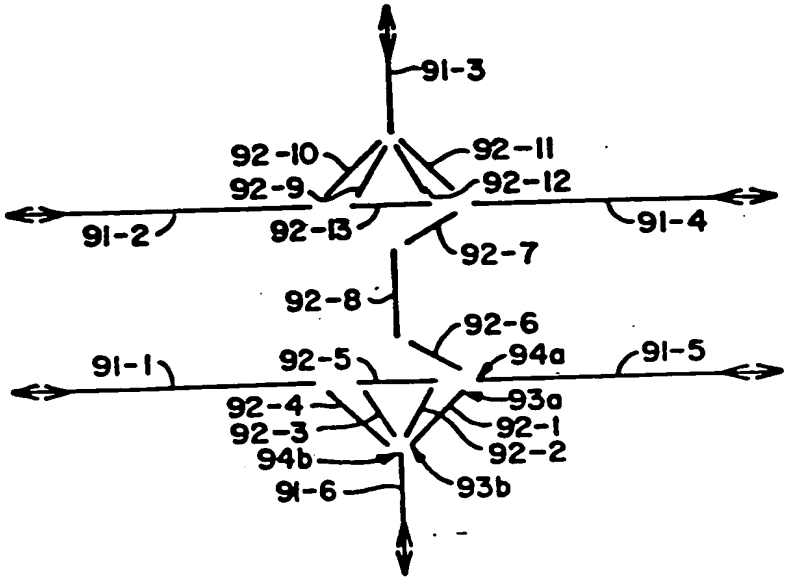


Figure 9B

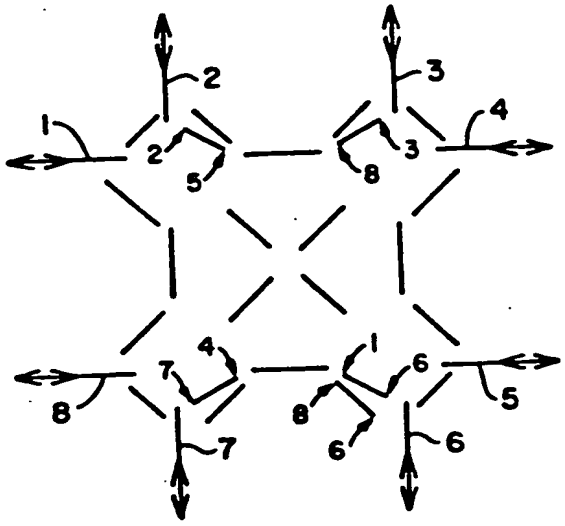


Figure 9C

Circled numbers on ends of pass devices indicate which paths are directly connected.

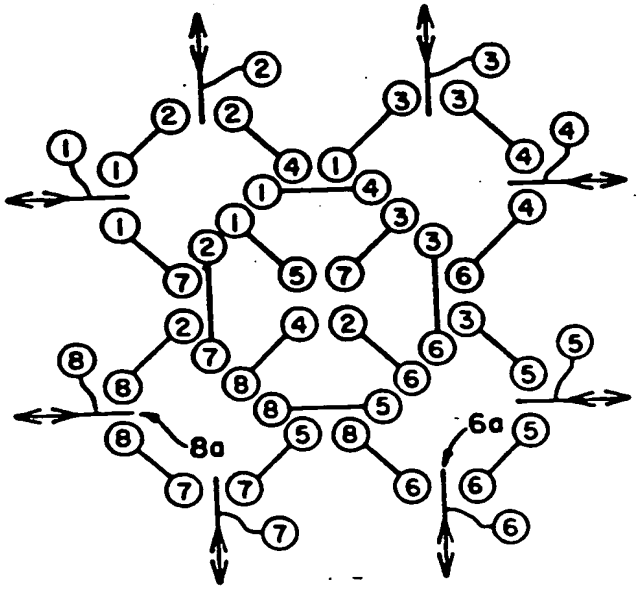


Figure 9D

Examples of possible connections with this method:

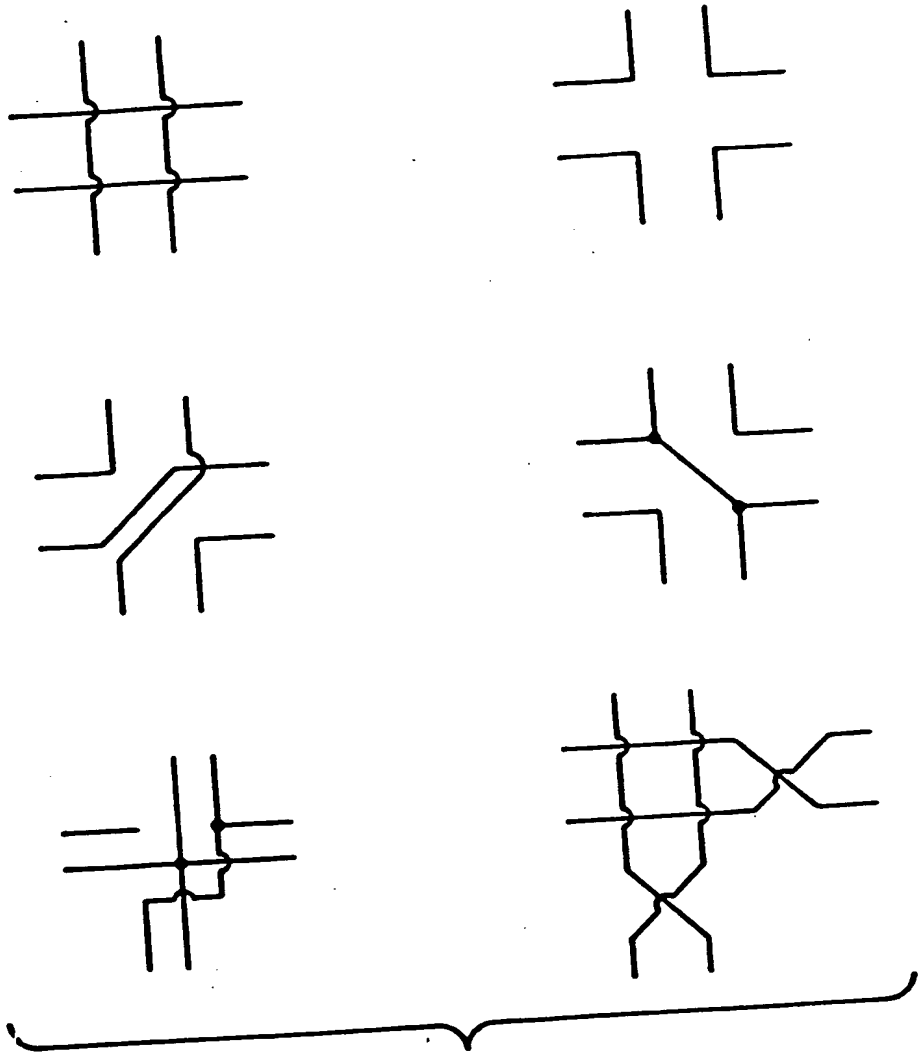


Figure 9E

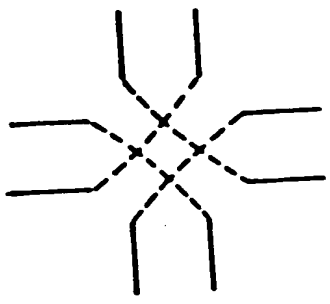


Figure 9F

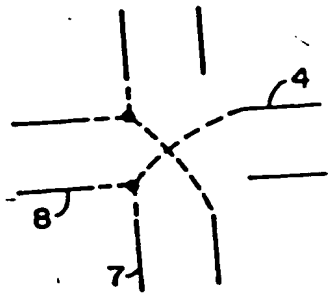


Figure 9G

BIDIRECTIONAL SELECTABLE BUFFER

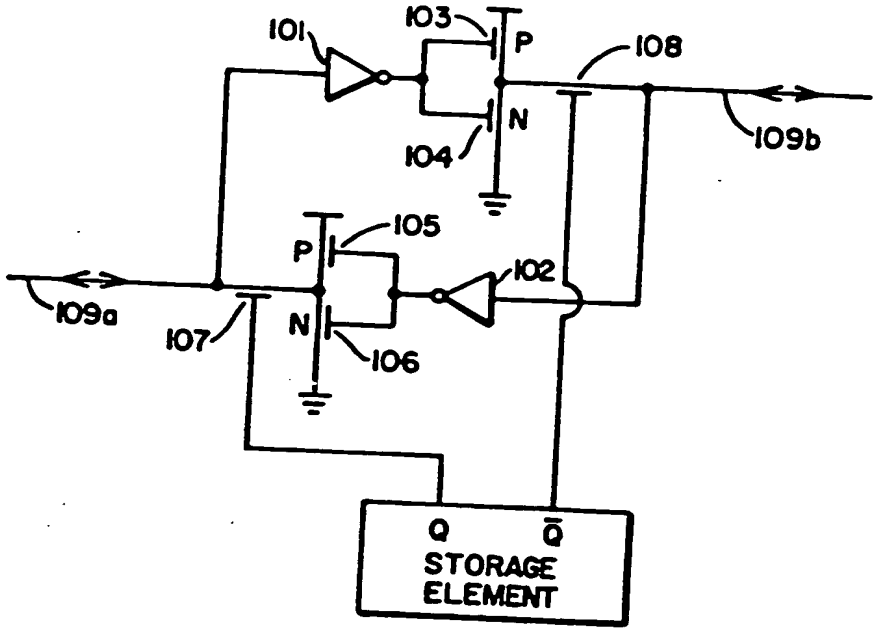


Figure 10A

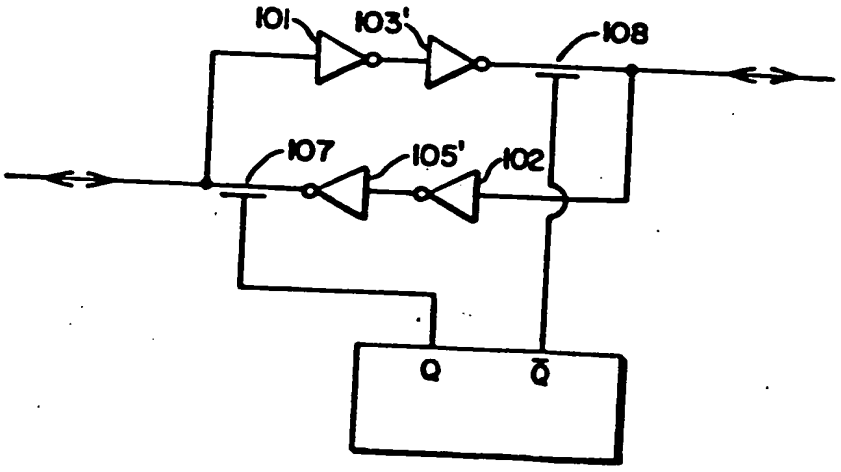
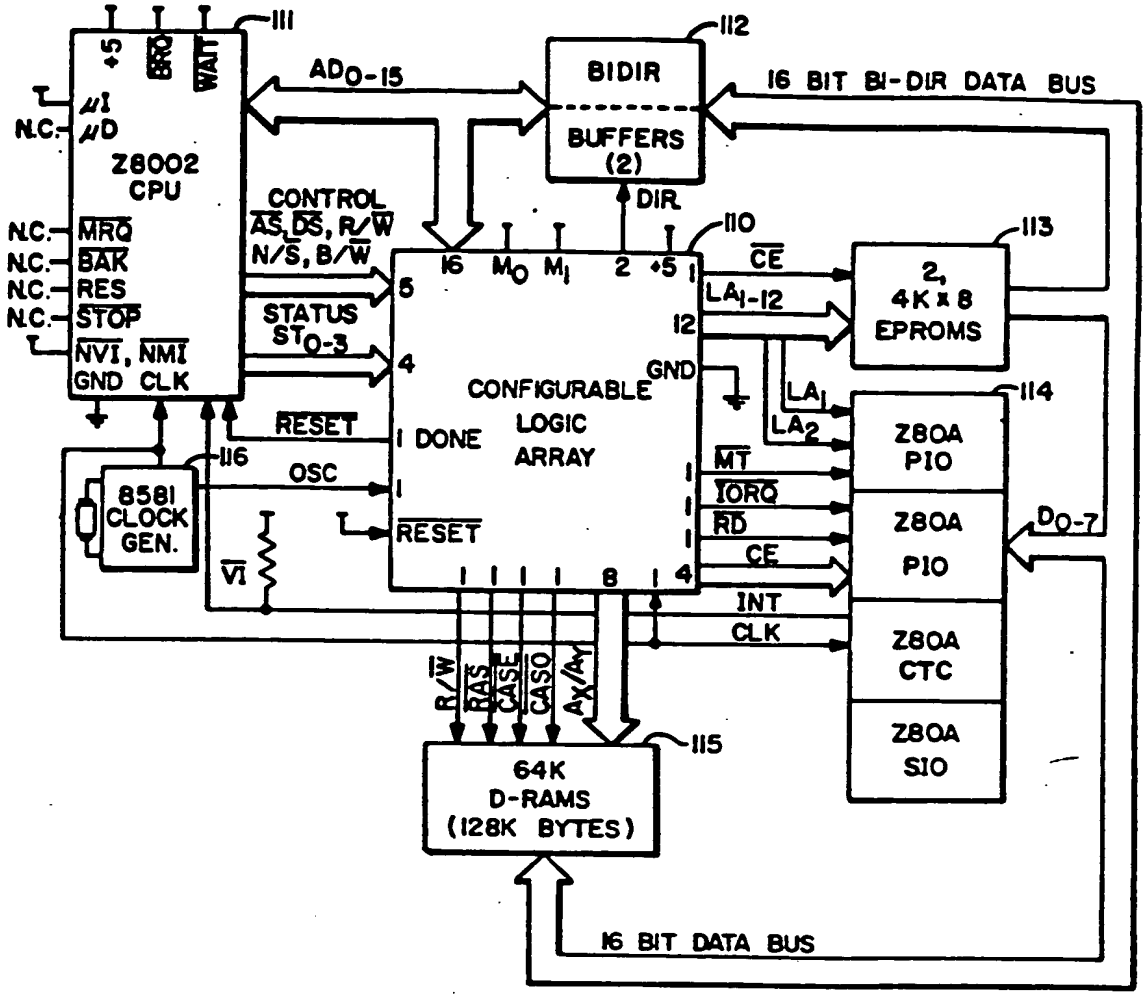


Figure 10B

Z8002 SINGLE BOARD μC



TTL SSI / MSI DESIGN

1 – CPU
2 – EPROMS
4 – LSI peripherals
16 – D-RAMS
1 – Clock generator
23 – TTL SSI / MSI

47 – Devices

CONFIGURABLE ARRAY DESIGN

1 – CPU
2 – EPROMS
4 – LSI peripherals
16 – D-RAMS
1 – Clock generator
2 – TTL SSI / MSI
1 – Configurable logic array

27 – Devices

Figure 11

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